

GERALD R. CLARK
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EDUCATION:

MS, Electrical Engineering, Electronic Circuits and Systems, [University of California San Diego](#), *Magna Cum Laude*, 1998. Completed as part of PhD work, Evolvable Hardware.

BS, Computer Engineering, Revelle College, Department of Electrical and Computer Engineering, University of California at San Diego, *Sum Cum Laude*, 1994.

EXPERIENCE:

Senior Systems Analyst, Talon Communications Q1 2007

Responsibilities included authoring the functional specification and technical documentation, completing the electrical schematic for the circuit card design of an MPEG-4 AVC encoder for a MIL-SPEC application. Technical challenges included a two-state heating/cooling system (sans fans) using complex thermoelectric cooling materials within a sealed chamber. The high-speed SMPTE 292M input along with other electrical interfaces, were magnetically and optically isolated for signal integrity optimization. KLV Metadata insertion and extraction were used to synchronize timing between video from various locations. All PES and TS headers and fields were managed in accordance with appropriate adopted industry standards. Central to the design was an FPGA-based solution with embedded/flexible cores for the microprocessor, the HDRX front-end logic using a built-in serial to parallel converter at 1.4GHz input rate. The unit could be field upgraded via a web-based interface using a combination of programmable flash banks and DDRII RAM.

Senior Technical Consultant, Sanko Holding: 2000-2006

Perform various consulting services and research and analysis in telecommunications sector for international client, [Sanko](#) Holding, Bursa Inegol, Turkey. As a board consultant to Sanko, identify and model paradigm shifts in market segments that represent high growth. Once modeled, analyzed, and approved, the programs and or products are used to serve the 225 Million Turkish-speaking peoples in several countries in Europe and Asia. Authored patent # 20020131130 on behalf of Sanko Holding, recently awarded in an international filing to protect telecommunication market interests in the Turkish deregulated telecommunications market.

Rolf Del Mar Private Holistic Health Care Practice, Nationally Certified HHP # 0505,

Holistic Health Care Practitioner (HHP) Business permit obtained in Del Mar, California June, 2005. Imaging equipment, analysis software, and various components of business established. Private practice information available from company website www.rolfdelmar.com

Guild for Structural Integration Certification Program Sept 2003-Nov 2004

Phase 1: Anatomy, Physiology, and Kinesiology: Boulder Colorado Sept 1-26, 2003

Jeff Linn and Andy Goodwin, Instructors

Phase 2: Auditor Phase, Kauai HI: Sept. 27-Nov 20 2003

Emmett Hutchins, Instructor

Phase 2 Deliverable: Submit graduation paper prior to Phase 3

[“Structure is Function and Energy”](#)

Phase 3: Practitioner Training, Kauai HI, Sept-Nov, 2004

2 clients through 10-series, Emmett Hutchins, Nilce Silvera Instructors

Vice President Engineering, [LightPointe](#), August 2000 – December 2002.

LightPointe designs and manufactures carrier-class optical transmission equipment using free-space optical (FSO) technology that delivers high-speed communications solutions to service providers. Responsibilities included leading a team of 40 worldwide engineers in the development and advancements of free-space optical products and microwave radio products for the ISM band and networking products. Worked closely with sales and marketing executives in defining corporate direction and developing relationships with telecommunications carriers like Qwest, MCI, Sprint, and the likes.

- Network architecture *secure* design & redundancy using FSO
- Patent on dynamic *secure* infrared wavelength translation
- Patent on multi-tenant unit wireless optical network distributed architecture (*secure* optical data distribution)
- Patent on all optical networks requiring no electro-optical conversion for IT and Network architectures.
- Secure, point-to-point Class 1M, 3B infrared laser communication equipment, design, test and manufacture

University of California, San Diego, Department of Electrical Engineering Aug 1993--Aug 1994

As an employee of UCSD engineering department, researched, prototyped, and presented research on a customer-funded multi-carrier spread spectrum *secure communications* system. Designed, prototyped, and modeled the adaptive multi-carrier spread spectrum communication system using mini-circuits functional elements (RF mixers, splitters, attenuators) and Labview for scope and simulation needs. PhD work continued under faculty advisor Dr. Paul Chau, Evolvable Hardware, with a completed prototype of the adaptive cellular array architecture FPGA. University research towards a PhD in Electrical engineering, having completed the academic coursework required for the PhD, while on sabbatical from Tiernan Communications as Director of Hardware Engineering.

Vice President Engineering, [Tiernan Communications](#), Dec 1996 – August 2000

Responsible for approximately 30 hardware and software development personnel in three separate markets: digital video broadcast, common carriers, and the Internet. Products developed for the broadcast included both standard and high definition digital television CODECs. The common carrier market was addressed using ATM and NMS equipment and software. Tiernan provided IP over DVB and data casting equipment for the Internet market.

As *Director, Hardware Engineering* for Tiernan, managed 25 junior & senior hardware engineers in the development of digital compression and decompression equipment for the commercial television broadcast market. As lead project engineer, developed multiple products and managed development teams from conception to manufacturing of final products. Technical duties were 80% while managerial duties were 20%.

While at Tiernan as a *Senior Engineer*, designed and implemented various video processing elements to include interpolation, decimation, and poly-phase filters. Algorithms were mapped to very large, flexible FPGAs as part of an MPEG-2 compression board. Developed various signal processing solutions for audio, video presentation and transport streams. VLSI Engineering Manager responsible for establishing the development platforms for

high volume commercial ASICs, submitting product ideas, staffing and managing funded projects.

Involved in all aspects of PCB design including schematic capture, programmable logic, placement, routing, fabrication, debug, and customer technical support. Schematic capture using Valid/Cadence graphical editors. Control logic development and modeling using Altera MaxPlusII and Cadence Design Systems.

Sr. Design Engineer, Lockheed Martin Telemetry and Instrumentation, Feb. 1995 - Jan 1997

Responsible for full PCB design for very high speed commercial and space based telecommunication applications. Schematic-capture and hardware modeling using VHDL, AHDL, and Verilog. Developed synchronous state machines, asynchronous receivers, control logic and re-sampling filters using both schematic and with HDL based methods. Altera 7000 and FLEX 10K devices used. Designed using Xilinx XC400E/L parts for digital designs. Designed and implemented various algorithms to include an N-Ary PSK Modulator, Cholesky matrix inversion, USART, asynchronous microprocessor interface, polyphase filters, and spectral processing functions. Designed and implemented an evolvable hardware algorithm in the Altera Apex 20K system on a chip.

Completed PCB board simulations and signal conditioning experience. Experienced with amplifiers, sensor interfaces and electro-mechanical device interfaces, through-hole and surface mount devices. FCC design methodology experience obtained for both class A and B products. Analog transmission line and clock skew analysis and modeling experience using LineSim. Various IBS models developed and used in simulation to optimize selection of discrete components to reduce clock skew and transmission line coupling and reflection. RF noise and signal conditioning experience compliant with FCC standards.

Project lead for DSP MODEM and RF up and down converter PCBs operating at 2.2 GHz for the Globalstar commercial satellite constellation. Developed the modulator, demodulator, bit synchronizer, and frame synchronizer for the MODEM using ANALOG Devices ADSP 2181 assembly and code.

Served as technical liaison at Lockheed Martin responsible for focusing research on SATCOM product development.

Involved in all aspects of the design, development, testing, and integration of the DSP and RF boards from both a hardware and software perspective.

Lead engineer responsible for Reed Solomon Channel Encoding and Decoding chip designed, modeled, and fabricated. Implemented programmable logic, DSP chip sets. Various modification made to the sequential algorithms for improved performance.

Systems Engineer, Reticular Systems Inc., Aug. 1989 - Feb. 1995

RSI was focused on using the Rotorcraft Pilot skills obtained in actual military service to create an expert system rule-base as part of a larger funding program under the Rotorcraft Pilot's Associate program administered by DARPA. Created a rule-base expert system and codified it in the C-Language Integrated Production System, (CLIPS), an artificial intelligence rule-based modeling language. This effort lead to an expert system microprocessor design that was based on the concept of parallel rules firing simultaneously in hardware that triggered the microprocessor fetch cycle. Designed and implemented a custom application specific integrated circuit (ASIC) using Mentor Graphics chip design software on a Sparc 20 workstation. Very high speed hardware description language (VHDL) was used to model the chip function and a laser programmable fabrication facility was identified to etch the first silicon.

Designed, implemented, tested, and documented hardware and software products. Authored proposals to various agencies and managed scheduled deliveries as project engineer. Skills acquired in CMOS VLSI and VHDL modeling, simulation, netlist synthesis and optimization, test vector generation, scan-chain insertion for JTAG 1193 test standards, technology mapping and optimization, layout and FPGA laser programmable chip fabrication.

Chief Warrant Officer, U.S. Army, Aviation Branch, Nov. 1982 – Aug. 1989

Pilot in command of AH1S Cobra Attack Helicopters and OH58 KIOWA A-C Observation Helicopters with approximately 1500 flight hours. Other duties included Night Vision & Instrumentation Trainer, and Master Fitness Trainer. Trained in secure military communications protocol to include meackoning, intrusion, jamming interference, and OPSEC. Trained extensively at the National Training Center, Bicycle Lake California. Multiple Integrated Laser Engagement Systems Training involving weapons systems modeling and transponder code tracking used to debrief pilots in the Starwars building where Tom Clancy garnered technical data for his best-selling novels. Duty locations/timelines follow:

1982-1983 Fort Rucker, Alabama: Army Helicopter Maintenance/Repair Training

1983-1884 128th Aviation Battalion, Chun Chon Korea

1984-1985 Fort Rucker, Alabama: Army Helicopter Flight Training Center

- AH-1 Cobra Qualification Training
- OH-58 Kiowa Transition Course
- OH-58 Aeroscout Nighthawk Training

1985-1987 Fort Riley, Kansas;

- 1/1 Attack Helicopter Battalion (AHB), Marshall Army Airfield:

Pilot In Command AH-1S Modified, Production, ECAS, 4 rotations NTC, Ft. Irwin, CA.

2 deployments approximately 1 month duration, Return of Forces to Germany (REFORGER)

1987-1989 Fort Riley, Kansas (outprocessing assignment)

- ¼ Air Cavalry, Marshall Army Airfield
- Pilot in Command OH-58 Kiowa helicopters with 1 rotation to NTC, Ft. Irwin, CA.

PATENTS:

20040120717: Extend Source Free-Space Optical Communication System

20020171896: Free-Space Optical Communication System Employing Wavelength Conversion

20020131130: Multi-Tenant Unit Optical Network

20020131130: Free-Space Optical Communications Network

20020131123: Terrestrial Optical Communication Network of Integrated Fiber and Free-Space which Requires no Electro-Optical Conversion

PUBLICATIONS:

Structure is Function and Energy, GSI, 2004.

Novel Evolvable Hardware Architectures within Modern FPGAs
CEC-99 Conference, Washington DC, 1999.

Digitizing American Television,
IMAPS-98 Conference, San Diego, CA 1998.

Dynamic Real-Time Constrained Evolvable Hardware

PhD. Preliminary Oral, University of California, San Diego, 1998.

Evolvable Hardware Control for Dynamic Reconfigurable and Adaptive Computing, 7th EP 1998 Conference, San Diego, CA, 1998.

Improved Concurrent Processing for Telemetry, International Telemetry Conference, San Diego, CA, 1996.

Enhanced Concurrent Processing for Improved Telemetry Performance, European Telemetry Conference, Garmisch, Germany, 1996.

Efficient Implementation for a VLSI Bi-directional Associative Memory, UCSD conference paper, 1995.

MEMBERSHIPS/Licenses:

- IEEE
- Optical Society San Diego
- Optical Society of America (OSA)
- Society of Photonics and Industrial Engineers (SPIE)
- Association of Bodywork and Massage Professionals: ABMP
- American Taekwondo Association : (ATA) Little Rock, AR, Rec. Black Belt
- Guild for Structural Integration: GSI, Boulder CO.
- National Certification for Therapeutic Massage and Bodywork Professionals
- Commercial Rotary Wing Instrument License
- Private Airplane, Single Engine Land, Instrument Ticket
- United States Hang Gliding Association (USHGA) Hang III